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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,312	04/18/2006	Johannus Leopoldus Bakx	NL 031238	9405

24737 7590 10/01/2009

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
CHU, KIM KWOK	

ART UNIT	PAPER NUMBER
2627	

MAIL DATE	DELIVERY MODE
10/01/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,312	BAKX, JOHANNUS LEOPOLDUS	
	Examiner	Art Unit	
	Kim-Kwok CHU	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Remarks on 7/13/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 April 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> *A person shall be entitled to a patent unless --*
> *(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.*

2. Claims 1-5 and 8-17 are rejected under 35 U.S.C. § 102(b) as being anticipated by Taniguchi (U.S. Patent 6,091,689).

3. Taniguchi teaches an optical detector system having all of the elements and means as recited in Claims 1-5, 8-14 and 16. For example, Taniguchi teaches the following:

Regarding Claim 1, the optical detector system (Figs. 7 and 12) comprising at least two optical detector units PD1, PD2 (Figs. 7 and 12) for receiving light generated from at least two lasers 4, respectively (Figs. 7 and 12; each laser source 4 has its respective LC1 and LC2; each LC1 and LC2 has photodetectors PD1 and PD2), each optical detector unit LC1/LC2 comprising an array of detector segments PD1, PD2 (Figs. 7 and 12) and at least one output terminal defining a current output of the corresponding optical detector unit (Fig. 7; the optical detector system is an integrated circuit having input/output circuits fabricated in a common substrate); and a signal

processing circuit 112 (Fig. 13; column 8; lines 50-54; a signal processing circuit is an operating means 112 for an optical disc system 100); wherein at least one current output (detector output) of a first optical detector unit LC1 is connected directly to a corresponding current output of a second optical detector unit LC2 at an output node 108, (Figs. 13; the optical detector system LC1/LC2 is an integrated circuit having input/output circuits such as current supplied/received circuits fabricated in a common substrate and connected to selector 108); the output node 108 being directly connected to a processing terminal 112 of the signal processing circuit 112 so that the processing terminal is directly connected to both the at least one current output of the first optical detector unit (LC1 .....LCn) and the corresponding current output of the second optical detector unit 102 (LC1 .....LCn), and wherein only a first detector unit LC1 of the at least two optical detector units is operative (Fig. 7; column 6, 1-6), as determined by an identity of a first laser 4 in use of the at least two lasers (Fig. 7), a second detector unit LC2 of the at least two optical detector units being non-operative by virtue of not receiving light from a second laser 4 of the at least two lasers so that an output of the second detector unit LC2 (Fig. 7) is floating (undetermined state), and does not affects output signals

produced by the first detector unit 4 (Fig. 7; column 5, lines 14-29).

Regarding Claim 2, the two optical detector units LC1, LC2 (Fig. 7) are of mutually identical design (Fig. 7; same semiconductor material).

Regarding Claim 3, the two optical detector units LC1, LC2 have mutually different wavelength sensitivity ranges (Fig. 7, column 5, lines 14-29).

Regarding Claim 4, each current output of the first optical detector unit LC1 is connected directly to the corresponding current output of the second optical detector unit LC2 at a corresponding output node (Fig. 7; two detectors belongs to the same integrated circuit).

Regarding Claim 5, the second optical detector unit LC2 in the non-operative state presents a high input impedance (Fig. 7; PD1/PD2 are not used and therefore no signal/current flowing).

Regarding Claim 8, the at least one input terminal comprises a current input (Fig. 13; inherent feature where input/output circuits in 102 carries current in form of a signal).

Regarding Claim 9, the one input terminal comprises a voltage input, and wherein a terminator resistor is connected to said line (Fig. 13; inherent feature where input/output circuits

use terminator resistors to limit currents as a form of a signals).

Regarding Claim 10, the terminator resistor is arranged in the proximity of the signal processing circuit 112 (Fig. 13).

Regarding Claim 11, the terminator resistor is integrated in an IC implementing the signal processing circuit 112 (Fig. 13; inherent feature where input/output circuits use terminator resistors to limit currents in an IC circuit as passive components).

Regarding Claim 12, light beam generating means 4 for generating at least two light beams (Fig. 7); optical components 2 (Fig. 2) for directing and focusing the two light beams in a focal spot on an optical disc 104 (Figs. 2 and 13); optical components 2 (Fig. 2) for directing reflected light beams to respective optical detector units LC1, LC2 of the optical detector system (Figs. 2 and 7).

Regarding Claim 13, the optical components 2 are arranged (reflects) such that the light beams have at least partly common light paths (Fig. 7; both light beams are reflected vertically in a partly common light path (Fig. 7; partly common light path is the light path where laser beams travel in a common vertical direction but partly overlapped as the light beams extend in a diverse form).

Regarding Claim 14, the optical components 2 are arranged such that the light beams have completely separate light paths (Fig. 7).

Regarding Claim 16, the disc drive apparatus 100 comprising an optical system according 102, 112 (Fig. 13).

4. Claims 15 and 17 have limitations similar to those treated in the above rejection, and are met by the reference as discussed above.

Response to Remarks

5. Applicant's Remarks filed on July 13, 2009 have been fully considered but they are not persuasive.

Applicant points out that the prior art (U.S. Patent 6,091,689) of Taniguchi's laser couplers LC1 to LCn are provided to the circuitry 112 (Figs. 12 and 13), where one of these outputs is selected by the selector 108 (page 11 of the Remarks, second paragraph). Therefore, Applicant argues that Taniguchi's photodiodes PD1, PD2 are not directly connected to each other at an output node, which is directly connected to a processing terminal (page 11 of the Remarks, lines 14-17). Accordingly, Applicant's detector outputs 60, 70 are directly connected to each other at an output node 81 (Fig. 3). Similarly, the prior art of Taniguchi's detector outputs LC1 to LCn are directly connected to each other (at the same input) at a node 108 (Fig. 13). With respect to the meaning of "directly connected to each other", Applicant's directly connected node 81 is illustrated in Fig. 9 where the signal/current of each detector's outputs are in fact a plurality of separated signal lines 81a to 81d. The plurality of signal lines 81a to 81d are directly connected to the processor 90. Similarly, the prior art of Taniguchi's detector outputs LC1 to LCn (Fig. 13) are a plurality of signals lines LC1 to LCn which are directly connected to the processor

112 at a common connector node 108. In this case, although the lines LC1 to LCn are directly connected to the processor 112 by a selector switch, the lines are still directly connected in a sense of multiplex mode. Therefore, this arrangement as Applicant described as "the circuitry 112 has multiple inputs to receive multiple outputs of the laser couplers LC1 to LCn" (page 11 of the Remarks, lines 11-13) is same as the inter-connection of Applicant's detector 60, 70 and signal processor 90 as illustrated in Fig. 4.

Furthermore, even Applicant's detector outputs 60, 70 are directly connected at one single node (line), the signal processor 90 still selects one output/signal among a plurality of outputs/signals to process from the single node 81 similar to the prior art of Taniguchi's selecting switch in the connecting node 108.

6. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Kim CHU whose telephone number is (571) 272-7585 between 9:30 am to 6:00 pm, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Nguyen, can be reached on (571) 272-7579.

The fax number for the organization where this application or proceeding is assigned is (571) 273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished application is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9191 (toll free).

/Kim-Kwok CHU/
Examiner AU2627
September 21, 2009
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/HOA T NGUYEN/

Supervisory Patent Examiner, Art Unit 2627